Laboratory 2 SPICE simulation following Extraction

Task 1(a)

The first task of this lab was to create a p-channel MOSFET with W' = 25µm and L' = 2µm with an n+ contact to the n-well so that the n-well can be biased to VDD. The design, DRC checker output and a cross sectional view including the bulk connection are shown below.

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|  | No errors were present. |
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Figure 1 Schematic Diagram, DRC Violations and Cross Sectional View of Layout

This layout contains two types of active regions: p+ and n+. In design terms the active regions (green) are defined as p+/n+ by a logic expression denoting the type of diffusion to take place over the active are. P-type diffusion (p-diff) or n-type diffusion (n-diff) respectively. The equation for P-diff is shown below:

N-diff = (ACTIVE) AND (NSELECT) AND (SUBS)

P-diff = (ACTIVE) AND (PSELECT) AND (NWELL)

We can see that the MOSFET is p-type as it’s active region is surrounded by a p-select (purple border) and inside a n-well (green border) hence there is a P-diff rectangle on top of the active region.

This circuit is now extracted as a SPICE file.

Task 1(b)

Before we can use this SPICE file in AIM-Spice we must make some alterations:

* The comments marked with a ‘\*’ were removed as they cluttered the file. This was not necessary but improved readability.
* Parser code from the L-Edit extraction started with a ‘.’ were removed as the specific codes do not parse correctly in AIM-Spice.
* The contents of “SNCA.SPC” were pasted into the top of the document. This contains parameters for a level 2 SCNA compliant simulation for NMOS and PMOS transistors.
* The model name was changed from “PMOS” to “CMOSP” so that it matched the model definition names in the SNCA file.
* The following voltage names were added: “VB 1 0 DC 5V”, “VGD 2 3”, “VSD 4 3” (explained later)

The resulting file is shown below.

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| .MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=417.000008E-10  + NSUB=6.108619E+14 VTO=0.825008 KP=4.919000E-05 GAMMA=0.172  + PHI=0.6 UO=594 UEXP=6.682275E-02 UCRIT=5000  + DELTA=5.08308 VMAX=65547.3 XJ=0.250000U LAMBDA=6.636197E-03  + NFS=1.98E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000  + RSH=32.740000 CGDO=3.105345E-10 CGSO=3.105345E-10 CGBO=3.848530E-10  + CJ=9.494900E-05 MJ=0.847099 CJSW=4.410100E-10 MJSW=0.334060 PB=0.800000  .MODEL CMOSP PMOS LEVEL=2 LD=0.227236U TOX=417.000008E-10  + NSUB=1.056124E+16 VTO=-0.937048 KP=1.731000E-05 GAMMA=0.715  + PHI=0.6 UO=209 UEXP=0.233831 UCRIT=47509.9  + DELTA=1.07179 VMAX=100000 XJ=0.250000U LAMBDA=4.391428E-02  + NFS=3.27E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000  + RSH=72.960000 CGDO=2.822585E-10 CGSO=2.822585E-10 CGBO=5.292375E-10  + CJ=3.224200E-04 MJ=0.584956 CJSW=2.979100E-10 MJSW=0.310807 PB=0.800000  M1 3 2 4 1 CMOSP L=2u W=25u AD=137.5p PD=61u AS=137.5p PS=61u  \* M1 DRAIN GATE SOURCE BULK (12 10 14 35)  VB 1 0 DC 5V  VGD 2 3  VSD 4 3 |

Figure Prepared SPICE file

The “\*M1…” comment was kept for clarity of the connection numbers. “VB 1 0 DC 5V” defines voltage “VB” at connection 1 (Bulk) compared to connection 0 (an implied connection to the ground) and sets it to a DC voltage of 5V (as specified in the worksheet). “VGD 2 3” defines voltage “VGD” at connection 2 (Gate) compared to connection 3 (Drain). “VSD 4 3” defines voltage “VSD” at connection 4 (Source) compared to connection 3 (Drain). Voltages are not given a value here. When parsed they are given a default value of DC 0V and changed later in a simulation.

This file is now pasted into AIM-Spice and saved as a circuit (.cir) file. A DC Transfer Curve Analysis was run with the first source being VSD with a range of 0V to -10V and steps in of -0.1V and a secondary source VGD with a range -1V to -5V and steps of -1V. Finally a output characteristic of i(vsd) was chosen. The output is shown below (Figure 3).

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Figure MOSFET output characteristics

This looks like the standard output characteristic mirrored vertically as VSD is negative.

Task 2

For task two we must create a CMOS inverter with dimensions 50λ high and 30λ wide with the largest transistors possible such that the inverter displays a symmetric voltage-transfer-curve (VTC) and using a slightly modified SCNA file "Scna\_r.spc".

The first step is to find the values for W/L which will create an electrically symmetric inverter. The equation for β is:

For an electrically symmetric device βp = βn.

In the model definition KP is equal to µ\*COX.

From Scna\_r: KPP = 2.45950E-05 and KPN = 4.919000E-05. Simplified:

So for electrical symmetry the PMOS must be twice the size.

The channel length (L) is the poly lines width. To double the PMOS ratio we can half LP with respect to LN or double WP­ with respect to WN the effect is similar. I have chosen to half LP so that both MOSFETs can take advantage of as much of the 30λ available width as possible for inversion channel length. This means LP will be 2λ, LN will be 4λ, WP = Wn hence theratio is preserved.

I will refer to L as the *poly width* from now to be consistent with L-Edit models and avoid confusion. Due to lack of available information a few assumptions were made: N-well, p-select and n-select can all extrude outside of the box. This is a fair assumption as the overlap rules are there to ensure correct doping profiles and if excess is lathed from the chip then no functionality should be lost; poly is not allowed to overlap as this may cause undesirable field effects (field fringing etc.); metal 1 and poly can extend but only if used for a connection